In the Claims:

Please amend the claims as follows:

1. (currently amended) A programming method for multilevel non-volatile memory cells comprising a first step wherein predetermined bias voltages are applied to the cell gate, drain and source terminals and providing a following control step of the programming just occurred by means of a programming algorithm of ~~the~~ a program-verify type, wherein the control step is skipped for some cells which have to reach a predetermined logic state.

2. (original) A method according to claim 1 wherein said predetermined logic state is the state "00".

3. (original) A method according to claim 1 wherein the control of said some cells is performed only after a part of the remaining cells has reached the programmed state.

4. (currently amended) A programming method for multilevel non-volatile memory cells comprising a first step wherein predetermined bias voltages are applied to the cell gate, drain and source terminals and providing a following control step of the programming just occurred by means of a programming algorithm of a program-verify type, wherein the control step is skipped for some cells which have to reach a predetermined logic state, ~~A method according to claim 1~~ and wherein the control step for said some cells is skipped by connecting to a ground potential reference the bit-line whereto these cells are connected.

5. (currently amended) A method according to claim 4 wherein it provides the use of a logic disabling network associated with ~~the~~ control circuit portions of the memory device.

6. (currently amended) A multilevel non-volatile memory electronic device integrated on a semiconductor and comprising a matrix of non volatile memory cells, each

cell being equipped with at least a floating gate transistor with gate, drain and source terminals, and comprising programming and control circuit portions associated with the cell matrix, wherein the control circuit portion comprises a logic network to disable ~~the reading~~ a control step only for some cells having to reach a predetermined logic state.

7. (original) A device according to claim 6 wherein said predetermined logic state is the state "00".

8. (currently amended) A device according to claim 6 wherein the control of said some cells is enabled only after a part of the remaining cells has reached the predetermined logic ~~programmed~~ state.

9. (currently amended) A multilevel non-volatile memory electronic device integrated on a semiconductor and comprising a matrix of non volatile memory cells, each cell being equipped with at least a floating gate transistor with gate, drain and source terminals, and comprising programming and control circuit portions associated with the cell matrix, wherein the control circuit portion comprises a logic network to disable a control step only for some cells having to reach a predetermined logic state, ~~A device according to claim 6~~ wherein the control of said some cells is disabled by connecting to a ground potential reference the bit-line whereto these cells are connected.

10. (previously presented) A method, comprising:

partially programming first and second multilevel non volatile memory cells having respective first and second states; and

determining the first state but not determining the second state.

11. (previously presented) The method of claim 10 wherein determining the first state comprises comparing the first state to a first predetermined value.

12. (previously presented) The method of claim 10 wherein determining the first state comprises determining whether the first state represents a first predetermined value.

13. (previously presented) The method of claim 10 wherein determining the first state comprises determining whether the first state represents a logic 01.

14. (previously presented) The method of claim 10 wherein determining the first state comprises determining whether the first state represents a logic 10.

15. (previously presented) The method of claim 10, further comprising repeating the partial programming and determining until the first state represents a first predetermined value.

16. (previously presented) The method of claim 10, further comprising:

repeating the partial programming and determining until the first state represents a first predetermined value; and

after the first state represents the first predetermined value, continuing to partially program the second memory cell but not the first memory cell.

17. (currently amended) The method of claim 10, further comprising:

repeating the partial programming and determining until the first state represents a first predetermined value;

after the first state represents the first predetermined value, partially programming the second memory cell but not the first memory cell;

~~after the first state represents the first predetermined value,~~ determining the second state of the second memory cell but not determining the first state of the first memory cell; and

repeating the partial programming of the second cell and the determining of the second state until the second state represents a second predetermined value.

18. (currently amended) The method of claim 10, further comprising:

repeating the partial programming and determining until the first state represents a first predetermined value;

after the first state represents the first predetermined value, partially programming the second memory cell but not the first memory cell;

~~after the first state represents the first predetermined value,~~ determining the second state of the second memory cell but not determining the first state of the first memory cell; and

repeating the partial programming of the second cell and the determining of the second state until the second state represents a logic 00.

19. (currently amended) The method of claim 10, further comprising:

repeating the partial programming and determining until the first state represents a first predetermined value;

after the first state represents the first predetermined value, partially programming the second memory cell but not the first memory cell;

~~after the first state represents the first predetermined value,~~ determining the second state of the second memory cell but not determining the first state of the first memory cell; and

repeating the partial programming of the second cell and the determining of the second state until the second state represents a fully programmed value.

20. (previously presented) An integrated circuit, comprising:

first and second multilevel non volatile memory cells having respective first and second states; and

programming circuitry coupled to the first and second memory cells and operable to,

provide respective programming pulses to the first and second memory cells, and

after providing the programming pulses, measure the first state but not the second state.

21. (previously presented) The integrated circuit of claim 20 wherein measuring the first state comprises determining whether the first state represents a first predetermined value.

22. (previously presented) The integrated circuit of claim 20 wherein the programming circuitry is further operable to sequentially provide additional respective

programming pulses and to measure the first state but not the second state until the first state represents a first predetermined value.

23. (previously presented) The integrated circuit of claim 20 wherein the programming circuitry is further operable to:

sequentially provide additional respective programming pulses and to measure the first state but not the second state until the first state represents a first predetermined value; and

after the first state represents the first predetermined value, to continue providing programming pulses to the second memory cell but not to the first memory cell.

24. (previously presented) The integrated circuit of claim 20 wherein the programming circuitry is further operable to:

sequentially provide additional respective programming pulses and to measure the first state but not the second state until the first state represents a first predetermined value; and

after the first state represents the first predetermined value, to sequentially provide programming pulses to the second memory cell but not to the first memory cell and measure the second state of the second memory cell but not the first state of the first memory cell until the second state represents a second predetermined value.

25. (previously presented) An electronic system, comprising:

an integrated circuit, comprising,

first and second multilevel non volatile memory cells having respective first and second states, and

programming circuitry coupled to the first and second memory cells and operable to,

provide respective programming pulses to the first and second memory cells, and

after providing the programming pulses, measure the first state but not the second state.